Claim(s):

1. A temporary storage device, comprising:

a first buffer, the first buffer configured to receive information, the information provided in association with a line clock signal, the first buffer configured to receive a first write enable signal for storing a first portion of the information;

a second buffer, the second buffer configured to receive the information, the information provided in association with the line clock signal, the second buffer configured to receive a second write enable signal for storing a second portion of the information different from the first portion of the information;

a system clock signal provided to the first buffer and the second buffer for synchronously clocking out the first portion and the second portion of the information; and

a pointer processor coupled to the first buffer to receive the first portion of the information, the pointer processor have a third buffer for storing the first portion of the information.

2. The temporary storage device of claim 1 further comprising coupled between the first buffer and the pointer processor, a first reader coupled to receive the first portion of the information from the first buffer and configured to provide a first read enable signal to the first buffer and to provide the first information to the poiner processor.

3. The temporary storage device of claim 2 further comprising:

combinatorial logic configured to provide the first write enable signal, the combinatorial logic configured to provide the first write enable signal in part when selected overhead signals are active;

an overhead extractor-processor configured to receive the second portion of the information; and

a second reader coupled between the overhead extractor-processor and the second buffer, the second reader coupled to receive the second portion of the information from the second buffer and configured to provide a second read enable

signal to the second buffer and to provide the second portion of the information to the overhead extractor-processor.

4. The temporary storage device of claim 1 wherein the first portion of the information synchronously outputted from the first buffer consists of H1-pointer, H2-pointer and H3-pointer information and a synchronous payload envelope.

5. The temporary storage device of claim 1 wherein the second portion of the information synchronously outputted from the second buffer consists of section overhead or line overhead or a combination thereof or consists of regenerator section or multiplex section overhead or a combination thereof.

6. The temporary storage device of claim 1 wherein the second write enable signal is a transport overhead signal or a section overhead signal.

7. The temporary storage device of claim 6 wherein the second write enable signal is active for providing available columns.

8. The temporary storage device of claim 1 wherein the first portion of the information or the second portion of the information is tagged.

9. The temporary storage device of claim 9 wherein the first portion of the information or the second portion of the information is tagged with an H1-pointer byte.

10. A network node comprising:

a receive line interface configured to receive at least one transmission;

buffers configured to decouple a line clock signal from input data and to couple a system clock signal to first and second output data; and

a pointer core coupled to receive the first output data from a first buffer of the buffers synchronous to the system clock signal, the pointer core having a pointer core associated buffer configured for synchronous operation with the system clock signal on an input and an output side.

11. The network node of claim 10 further comprising:

an overhead extractor-processor coupled to receive the second output data from a second buffer of the buffers synchronous to the system clock signal.

12. The network node of claim 11 further comprising:

a first multiplexer coupled to receive the first output data from the first buffer and to provide the first output data to the pointer core; and

a second multiplexer coupled to receive the second output data from the second buffer and to provide the second output data to the overhead extractor processor.

13. The network node of claim 12 wherein the multiplexers are round-robin readers clocked by the system clock signal.

14. A network node comprising:

a frame timing generator, the frame timing generator configured for synchronous operation off of a system clock signal;

a temporary storage device configured to receive data output from the frame timing generator, the temporary storage device configured to decouple the system clock signal from the data and to couple a line clock signal to the data, the data written to the temporary storage device synchronous to the system clock signal, the data outputted from the temporary storage device synchronous to the line clock signal; and

a pointer core having a buffer, the buffer configured to receive the data output from the temporary storage device, the buffer configured to operate on both an input side and an output side synchronous with the line clock signal.

15. A network comprising:

a first network node;

a second network node;

a communication link for putting the first network node in communication with the second network node;

the first network node configured with a receive buffer, the receive buffer

comprising:

a first buffer, the first buffer configured to receive at least a first portion of the overhead information, the at least a first portion of the overhead information provided in association with a line clock signal, the first buffer configured to store a first portion of the at least a first portion of the overhead information; and

a second buffer, the second buffer configured to receive at least a second portion of the overhead information, the at least a second portion of the overhead information provided in association with a line clock signal, the second buffer configured to store a second portion of the at least a second portion of the overhead information.

16. The network of claim 15 wherein the receive buffer is located on an input data path in advance of a pointer processor buffer.

17. A method for avoiding one or more asynchronicities in pointer processing, comprising:

providing a first buffer and a second buffer;

providing a frame structure clocked to a line clock to the first buffer;

providing the frame structure clocked to the line clock to the second buffer;

storing a first portion of the frame structure in the first buffer;

storing a second portion of the frame structure in the second buffer, the second portion different from the first portion;

clocking out the first portion of the frame structure from the first buffer synchronous to a system clock signal;

clocking out the second portion of the frame structure from the second buffer synchronous to the system clock signal;

providing the first portion and the second portion of the frame structure from the first buffer and the second buffer to a pointer processor buffer; and

clocking out with a pulse signal synchronized with the system clock signal the first portion and the second portion of the frame structure from the pointer processor buffer.

18. A network comprising:

a first network node;

a second network node;

a communication link for putting the first network node in communication with the second network node;

the first network node configured with a receive buffer and a transmit buffer, the transmit buffer comprising:

a frame timing generator; and

a temporary storage device configured to receive data output from the frame timing generator, the temporary storage device configured to decouple a system clock signal from the data and to couple a line clock signal to the data, the data written to the temporary storage device synchronous to the system clock signal and outputted from the temporary storage device synchronous to the line clock signal.

19. The network of claim 18 wherein the transmit buffer is located on an input data path in advance of a pointer processor buffer.

20. A temporary storage device configured to receive overhead information and data, comprising:

a first buffer, the first buffer coupled to receive at least a first portion of the overhead information, the at least a first portion of the overhead information provided in association with a line clock signal, the first buffer configured to store the at least a first portion of the overhead information to provide first stored overhead information;

a second buffer, the second buffer coupled to receive at least a second portion of the overhead information, the at least a second portion of the overhead information provided in association with the line clock signal, the second buffer configured to store

the at least a second portion of the overhead information to provide second stored ovehead information; and

the first buffer and the second buffer coupled to receive a system clock signal and configured to respectively clock out the first and second stored information synchronous to the system clock signal.

21. The temporary storage device of claim 20 further comprising:

a pointer processor coupled to receive the first stored overhead information, the pointer processor have a third buffer for storing the first stored overhead information.

22. The temporary storage device of claim 21 further comprising a first reader coupled to receive the first stored overhead information from the first buffer and configured to provide a first read enable signal to the first buffer and to provide the first stored overhead information to the poiner processor.

23. The temporary storage device of claim 22 further comprising first combinatorial logic configured to provide a first write enable signal to select the at least a first portion of the overhead information written to the first buffer.

24. The temporary storage device of claim 23 further comprising an overhead extractor-processor coupled to receive the second stored overhead information.

25. The temporary storage device of claim 24 further comprising a second reader coupled to receive the second stored overhead information from the second buffer and configured to provide a second read enable signal to the second buffer and to provide the second stored overhead information to the overhead extractor-processor.

26. The temporary storage device of claim 25 further comprising second combinatorial logic configured to provide a second write enable signal to select the at least a second portion of the overhead information written to the second buffer.